UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,810	12/09/2003	Stephen Li	TI-36016	4341

23494 7590 07/19/2007
TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
MAGLO, EMMANUEL K	

ART UNIT	PAPER NUMBER
2609	

NOTIFICATION DATE	DELIVERY MODE
07/19/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@ti.com
uspto@dlemail.itg.ti.com

Office Action Summary	Application No.	Applicant(s)	
	10/731,810	LI ET AL.	
	Examiner	Art Unit	
	Emmanuel Maglo	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

CHARLES D. GARBER
SUPERVISORY PATENT EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *None*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-21 are rejected under 35 U.S.C 103(a) as been unpatentable over Griesmer et al. (5,555,405), hereinafter referred to as Griesmer, in view of Lavigne (US 6,954,812), hereinafter referred to as Lavigne.

Regarding claim 1, Griesmer discloses a plurality of data queues, herein called free queues (column 5 lines 1-15, and Fig. 5 elements 75a, 75b...75n); an arbitration table, herein called forwarding table (column 7 lines 59-60, and Fig. 3, element 70) comprising a plurality of entries, herein called forwarding entry sets (column 7 lines 60-62, and Fig. 3, element 72 composed of FES1, FES2, FES3...); empty flags from each of the data queues, the flags indicating that there is no data to the sent from that queue (flags or status flags corresponding to free space segments as show in Fig. 3 elements

73: FSS1, FSS3..., and in Fig.4, where $FSS_{k\ (k\ is\ between\ 1\ and\ n)}$ and (column 7 lines 56-67) are received from the data queues).

Griesmer does not explicitly teach a first multiplexer receiving an output from a first table entry and an output from a second table entry in the arbitration table or a second multiplexer receiving empty flags from each of the data queues, the flags indicating that there is no data to the sent from that queue, an output of the second multiplexer being coupled to a control input of the first multiplexer whereby the first table entry value is output from the first multiplexer if the corresponding queue has data to be sent out and the second table entry value is sent out from the first multiplexer if the queue corresponding to that table entry has data to be sent out and the queue corresponding to the first entry has no data to be sent out.

Lavigne, in the same field of endeavor, in the same field of endeavor discloses an arbitrator system comprising an arbitrator logic circuit (Fig. 1) a first multiplexer (Fig. 2 (continued) Mux1) receiving an output from a first table entry and an output from a second table entry in the arbitration table, and a second multiplexer (Fig. 2 (continued) Mux2) receiving empty flags from each of the data queues, a module 10 and a module 20 of Fig. 1 to process the separate subsections of the table entries. Once the Arbiter1 of module 10 generates a new selection, that new selection is inputted into the first multiplexer or MUX1 and coupled to other signal to produce the input to the second multiplexer or MUX2. Output of MUX2 is then inputted into MUX1 (columns 3 and 4 lines 64-67 and 1-8, respectively)

It would have been obvious to one having ordinary skill in the art at the time the

invention was made to modify Griesmer's teaching by incorporating the teaching of Lavigne to connect to arbitration system 100 to use the first multiplexer and the second multiplexer

The motivation is to reduce the processing cycle because, by collecting data from the subtending transmission devices round robin arbitration typically entails choosing elements or entries of a table or a set in a way that describes some sort of cyclical successive approximation, and would involve many logic gates processing.

Regarding claim 2, and as applied to claim 1 above, Griesmer discloses an arbitrator wherein the second table entry is in juxtaposition to the first table entry (Fig. 5 elements 90a-90z are in juxtaposition to 70a-70z); where the number of entries in the table varies between a and z.

Regarding claim 3, and as applied to claim 1 above, Griesmer discloses the entries of the tables herein called forwarding entry sets (column 7 lines 60-62, and Fig. 3, element 72 composed of FES1, FES2, and FES3...)

Griesmer does not explicitly teach the entries of the tables to be between 32 and 256. Lavigne, in the same field of endeavor, teaches that the arbitrator can arbitrate among 256 entries (herein referred to as requests column 3 lines 33-35), of the tables where (column 2 lines 44 and 45) one of the stages generates a signal to synchronize the operation of the first stage and the second stage.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Griesmer's teaching by incorporating the teaching of Lavigne to set the number of entries in the tables between 32-256, and to connect such

tables to the arbitrators, so that output of module 20 is fed as a signal to the first stage module 10 and to the second module 20 (column 3 lines19-22).

The motivation is to reduce the processing cycle because, by collecting data from the subtending transmission devices round robin arbitration typically entails choosing elements or entries of a table or a set in a way that describes some sort of cyclical successive approximation, and would involve many logic gates processing

Regarding claim 4, and as applied to claim 1 above, Griesmer does not explicitly teach data selection from the table corresponding to queue with has data to be send out.

Lavigne, in the same field of endeavor, teaches data selected from the table corresponds to that which has valid queue entry, because the second multiplexer selects the active request from selected block to generate new selections (column 4 lines 30-34).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Griesmer's teaching by incorporating the teaching of Lavigne to send data from tables in the corresponding queues if data is present.

The motivation is to design a true round robin arbitrator system by reducing the logic circuits involved in the cyclical processing (column 1 lines 34-46).

Regarding claim 5, and as applied to claim 1 above, Griesmer discloses the claimed invention except the separate processing of the subsections.

Lavigne, in the same field of endeavor, teaches separate processing of subsections of the table entries, using the first arbiter then the second, as table entries partition into a plurality of blocks requests, (column 5 lines 38-47).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Griesmer's teaching by incorporating the teaching of Lavigne to set bit width of Arbiter1 and Arbiter2 to the desired bit width for the arbitration system.

The motivation is to use one or more active requests to generate the first index associated to the selected block, so that that the selection of the particular block and the selection of the active request of the particular block are synchronized to output a valid signal.

Regarding claim 6, and as applied to claim 5 above, Griesmer discloses the claimed invention except the carry-look-ahead circuit used to select the next entry in the table.

Lavigne, in the same field of endeavor, teaches the carry-look-ahead circuit used to select the next table entry after a valid signal is outputted, causing the index to be maintained "High".

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Griesmer's teaching by incorporating the teaching of Lavigne

The motivation is that for the valid signal selection, module 2 must select active request bits from the previously selected block, a sort of pointer to the next the pre-selected entry.

Regarding claim 7, and as applied to claim 6 above, Griesmer discloses the claimed invention except ANDing empty flags of each subsection to generate empty signal except the use of the resulting subsection empty signal to route the second input into the first multiplexer.

Lavigne, in the same field of endeavor, teaches the round robin arbitration system comprising an arbitrator logic circuit (Fig. 1), a first multiplexer (Fig. 2 (continued) Mux1) receiving an output from a first table entry and an output from a second table entry in the arbitration table, and a second multiplexer (Fig. 2 (continued) Mux2) receiving empty flags from each of the data queues, a module 10 and a module 20 of Fig. 1 to process the separate subsections of the table entries that are inputted into the AND gate (column 5 lines 1-4, and Fig. 2 continued element 270). The multiplexing of the empty flags of the subsections necessary generates the subsection empty signal that is in turn routed to the first multiplexer, after being outputted from the second.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Griesmer's teaching by incorporating the teaching of Lavigne to AND together the empty flags to produce the empty signal, and to use the resulting subsection empty signal to route the second input to the first.

The motivation is that use one or more active requests to generate the first index associated to the selected block, so that the selection of the particular block and the

selection of the active request of the particular block are synchronized to reduce the processing cycle for the design a of true round robin arbitration system. In that regards for a valid signal selection, active request of the particular block must be initiated.

Regarding claim 8, and as applied to claim 1 above, Griesmer discloses the claimed invention except that the entries in the table are rotated in position after each time slot.

Lavigne, in the same field of endeavor, teaches the round robin arbitration system wherein the table entry that is sent out is rotated to the end of the table and all slots between this slot and the end of the table are rotated by one position; because each entry or valid signal is represented by a time slot for the transmission of one data packet, the valid signal prevents the same active request to be send two cycles in a row (column 4 lines 59-66).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Griesmer's teaching by incorporating the teaching of Lavigne.

The motivation is that the round robin arbitration system **100** produces true round robin results, one every cycle. And once a result is produced for an entry the cycle is ended and a new cycle starts with the next or subsequent entry such that entries in the table are rotated in position after each cycle.

Regarding claim 9, and as applied to claim 1 above, Griesmer discloses the claimed invention except that the data is sent out from one of the data queues during each clock cycle.

Lavigne teaches a system where data is sent out from the data queues during each clock cycle (column 2 lines 56-58), because one stage generates a signal to synchronize the operation of the first and the second stage.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Griesmer's teaching by incorporating the teaching of Lavigne to connect to arbitration system 100 to use the first multiplexer and the second multiplexer to produce true round robin results, one result every cycle.

The motivation is that to produce true round robin results, one result every cycle, it is necessary to reduce the processing cycle because of the many logic circuits involved. By collecting data from the subtending transmission devices, round robin arbitration typically entails choosing elements or entries of a table or a set in a way that describes some sort of cyclical successive approximation, and would involve many logic gates processing.

Regarding claim 10, Griesmer does not explicitly teach data selection from the table corresponding to queue with has data to be send out.

Lavigne, in the same field of endeavor, teaches data selected from the table corresponds to that which has valid queue entry, because the second multiplexer selects the active request from selected block to generate new selections (column 4 lines 30-34).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Griesmer's teaching by incorporating the teaching of Lavigne to send data from tables in the corresponding queues if data is present.

The motivation is to design a true round robin arbitrator system by reducing the logic circuits involved in the cyclical processing (column 1 lines 34-46).

Regarding claim 11, and as applied to claim 10 above, Griesmer does not explicitly teach data selection from the table corresponding to queue with has data to be send out.

Lavigne, in the same field of endeavor, teaches data selected from the table corresponds to that which has valid queue entry, because the second multiplexer selects the active request from selected block to generate new selections (column 4 lines 30-34).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Griesmer's teaching by incorporating the teaching of Lavigne to send data from tables in the corresponding queues if data is present.

The motivation is to design a true round robin arbitrator system by reducing the logic circuits involved in the cyclical processing (column 1 lines 34-46).

Regarding claim12, and as applied to claim 10 above, Griesmer discloses the claimed invention except the separate processing of the subsections.

Lavigne, in the same field of endeavor, teaches separate processing of subsections of the table entries, using the first arbiter then the second, as table entries partition into a plurality of blocks requests, (column 5 lines 38-47).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Griesmer's teaching by incorporating the teaching of

Lavigne to set bit width of Arbiter1 and Arbiter2 to the desired bit width for the arbitration system.

The motivation is to use one or more active requests to generate the first index associated to the selected block, so that that the selection of the particular block and the selection of the active request of the particular block are synchronized to output a valid signal.

Regarding claim 13, and as applied to claim 12 above, Griesmer discloses the claimed invention except the carry-look-ahead circuit used to select the next entry in the table.

Lavigne, in the same field of endeavor, teaches the carry-look-ahead circuit used to select the next table entry after a valid signal is outputted, causing the index to be maintained "High".

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Griesmer's teaching by incorporating the teaching of Lavigne

The motivation is that for the valid signal selection, module 2 must select active request bits from the previously selected block, a sort of pointer to the next the pre-selected entry.

Regarding claim 14, and as applied to claim 13 above, Griesmer discloses the claimed invention except ANDing empty flags of each subsection to generate empty signal except the use of the resulting subsection empty signal to route the second input into the first multiplexer.

Lavigne, in the same field of endeavor, teaches the round robin arbitration system comprising an arbitrator logic circuit (Fig. 1), a first multiplexer (Fig. 2 (continued) Mux1) receiving an output from a first table entry and an output from a second table entry in the arbitration table, and a second multiplexer (Fig. 2 (continued) Mux2) receiving empty flags from each of the data queues, a module 10 and a module 20 of Fig. 1 to process the separate subsections of the table entries that are inputted into the AND gate (column 5 lines 1-4, and Fig. 2 continued element 270). The multiplexing of the empty flags of the subsections necessary generates the subsection empty signal that is in turn routed to the first multiplexer, after being outputted from the second.
It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Griesmer's teaching by incorporating the teaching of Lavigne to AND together the empty flags to produce the empty signal, and to use the resulting subsection empty signal to route the second input to the first.
The motivation is that use one or more active requests to generate the first index associated to the selected block, so that the selection of the particular block and the selection of the active request of the particular block are synchronized to reduce the processing cycle for the design a of true round robin arbitration system. In that regards for a valid signal selection, active request of the particular block must be initiated.

Regarding claim 15, and as applied to claim 11 above, Griesmer discloses the claimed invention except the separate processing of the subsections.

Lavigne, in the same field of endeavor, teaches separate processing of subsections of the table entries, using the first arbiter then the second, as table entries partition into a plurality of blocks requests, (column 5 lines 38-47).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Griesmer's teaching by incorporating the teaching of Lavigne to set bit width of Arbiter1 and Arbiter2 to the desired bit width for the arbitration system.

The motivation is to use one or more active requests to generate the first index associated to the selected block, so that that the selection of the particular block and the selection of the active request of the particular block are synchronized to output a valid signal.

Regarding claim 16, and as applied to claim 11 above, Griesmer discloses the claimed invention except the carry-look-ahead circuit used to select the next entry in the table.

Lavigne, in the same field of endeavor, teaches the carry-look-ahead circuit used to select the next table entry after a valid signal is outputted, causing the index to be maintained "High".

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Griesmer's teaching by incorporating the teaching of Lavigne

The motivation is that for the valid signal selection, module 2 must select active request bits from the previously selected block, a sort of pointer to the next the pre-selected entry.

Regarding claim 17, and as applied to claim 10 above, Griesmer discloses the claimed invention except the carry-look-ahead circuit used to select the next entry in the table.

Lavigne, in the same field of endeavor, teaches the carry-look-ahead circuit used to select the next table entry after a valid signal is outputted, causing the index to be maintained "High".

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Griesmer's teaching by incorporating the teaching of Lavigne

The motivation is that for the valid signal selection, module 2 must select active request bits from the previously selected block, a sort of pointer to the next the pre-selected entry.

Regarding claim 18, and as applied to claim 10 above, Griesmer discloses the claimed invention except ANDing empty flags of each subsection to generate empty signal except the use of the resulting subsection empty signal to route the second input into the first multiplexer.

Lavigne, in the same field of endeavor, teaches the round robin arbitration system comprising an arbitrator logic circuit (Fig. 1), a first multiplexer (Fig. 2 (continued) Mux1) receiving an output from a first table entry and an output from a second table

entry in the arbitration table, and a second multiplexer (Fig. 2 (continued) Mux2) receiving empty flags from each of the data queues, a module 10 and a module 20 of Fig. 1 to process the separate subsections of the table entries that are inputted into the AND gate (column 5 lines 1-4, and Fig. 2 continued element 270). The multiplexing of the empty flags of the subsections necessary generates the subsection empty signal that is in turn routed to the first multiplexer, after being outputted from the second.
It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Griesmer's teaching by incorporating the teaching of Lavigne to AND together the empty flags to produce the empty signal, and to use the resulting subsection empty signal to route the second input to the first.
The motivation is that use one or more active requests to generate the first index associated to the selected block, so that the selection of the particular block and the selection of the active request of the particular block are synchronized to reduce the processing cycle for the design a of true round robin arbitration system. In that regards for a valid signal selection, active request of the particular block must be initiated.

Regarding claim 19, and as applied to claim 11 above, Griesmer discloses the claimed invention except ANDing empty flags of each subsection to generate empty signal except the use of the resulting subsection empty signal to route the second input into the first multiplexer.
Lavigne, in the same field of endeavor, teaches the round robin arbitration system comprising an arbitrator logic circuit (Fig. 1), a first multiplexer (Fig. 2 (continued) Mux1) receiving an output from a first table entry and an output from a second table

entry in the arbitration table, and a second multiplexer (Fig. 2 (continued) Mux2) receiving empty flags from each of the data queues, a module 10 and a module 20 of Fig. 1 to process the separate subsections of the table entries that are inputted into the AND gate (column 5 lines 1-4, and Fig. 2 continued element 270). The multiplexing of the empty flags of the subsections necessary generates the subsection empty signal that is in turn routed to the first multiplexer, after being outputted from the second.
It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Griesmer's teaching by incorporating the teaching of Lavigne to AND together the empty flags to produce the empty signal, and to use the resulting subsection empty signal to route the second input to the first.
The motivation is that use one or more active requests to generate the first index associated to the selected block, so that the selection of the particular block and the selection of the active request of the particular block are synchronized to reduce the processing cycle for the design a of true round robin arbitration system. In that regards for a valid signal selection, active request of the particular block must be initiated.

Regarding claim 20, and as applied to claim 12 above, Griesmer discloses the claimed invention except ANDing empty flags of each subsection to generate empty signal except the use of the resulting subsection empty signal to route the second input into the first multiplexer.
Lavigne, in the same field of endeavor, teaches the round robin arbitration system comprising an arbitrator logic circuit (Fig. 1), a first multiplexer (Fig. 2 (continued) Mux1) receiving an output from a first table entry and an output from a second table

entry in the arbitration table, and a second multiplexer (Fig. 2 (continued) Mux2) receiving empty flags from each of the data queues, a module 10 and a module 20 of Fig. 1 to process the separate subsections of the table entries that are inputted into the AND gate (column 5 lines 1-4, and Fig. 2 continued element 270). The multiplexing of the empty flags of the subsections necessary generates the subsection empty signal that is in turn routed to the first multiplexer, after being outputted from the second.
It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Griesmer's teaching by incorporating the teaching of Lavigne to AND together the empty flags to produce the empty signal, and to use the resulting subsection empty signal to route the second input to the first.
The motivation is that use one or more active requests to generate the first index associated to the selected block, so that the selection of the particular block and the selection of the active request of the particular block are synchronized to reduce the processing cycle for the design a of true round robin arbitration system. In that regards for a valid signal selection, active request of the particular block must be initiated.

Regarding claim 21, and as applied to claim 1 above, Griesmer discloses the claimed invention except that the entries in the table are rotated in position after each time slot.
Lavigne, in the same field of endeavor, teaches the round robin arbitration system wherein the table entry that is sent out is rotated to the end of the table and all slots between this slot and the end of the table are rotated by one position; because each entry or valid signal is represented by a time slot for the transmission of one data

packet, the valid signal prevents the same active request to be send two cycles in a row (column 4 lines 59-66).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Griesmer's teaching by incorporating the teaching of Lavigne.

The motivation is that the round robin arbitration system **100** produces true round robin results, one every cycle. And once a result is produced for an entry the cycle is ended and a new cycle starts with the next or subsequent entry such that entries in the table are rotated in position after each cycle.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Maglo whose telephone number is (571)270-1854. The examiner can normally be reached on Monday - Friday 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on (571)270-1202. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

E.M.

Yuwen Pan

CHARLES D. GARBER
SUPERVISORY PATENT EXAMINER